Notes for course EE1.1 Circuit Analysis 2004-05

TOPIC 9 – OPERATIONAL AMPLIFIER AND TRANSISTOR CIRCUITS

- Op-amp basic concepts and sub-circuits
- Practical aspects of op-amps; feedback and stability
- Nodal analysis of op-amp circuits
- Transistor models
- Frequency response of op-amp and transistor circuits

1 THE OPERATIONAL AMPLIFIER: BASIC CONCEPTS AND SUB-CIRCUITS

1.1 General

The operational amplifier is a universal active element

It is cheap and small and easier to use than transistors

It usually takes the form of an integrated circuit containing about 50 – 100 transistors; the circuit is designed to approximate an ideal controlled source; for many situations, its characteristics can be considered as ideal

It is common practice to shorten the term "operational amplifier" to op-amp

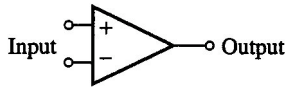
The term operational arose because, before the era of digital computers, such amplifiers were used in analog computers to perform the operations of scalar multiplication, sign inversion, summation, integration and differentiation for the solution of differential equations

Nowadays, they are considered to be general active elements for analogue circuit design and have many different applications

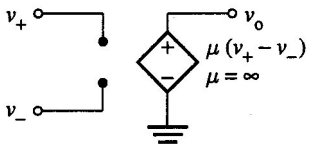
1.2 Op-amp Definition

We may define the op-amp to be a grounded VCVS with a voltage gain (μ) that is infinite

The circuit symbol for the op-amp is as follows:



An equivalent circuit, in the form of a VCVS is as follows:



The three terminal voltages v_+, v_-, and v_o are all node voltages relative to ground

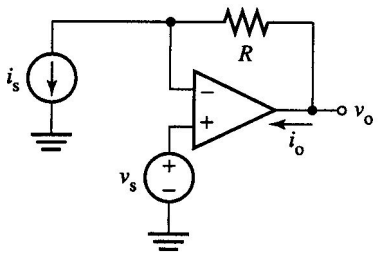
When we analyze a circuit containing op-amps, we cannot use the constraint equation $\mu(v_+ - v_-)$ since the gain μ is infinite

This property requires a different approach to the analysis of op-amp circuits

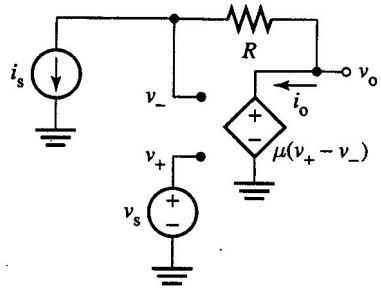
1.3 The Op-amp Virtual Short Model

We first assume that μ is finite, perform analysis in the conventional way, and then allow μ to tend to infinity

Consider the following simple op-amp circuit; we wish to determine the output voltage v_o:



We can replace the op-amp symbol with its infinite voltage gain VCVS equivalent and then denote the gain by a finite parameter μ:



We can apply KCL, bearing in mind that no current flows into the op-amp input terminals (they are equivalent to an open circuit):

$$\frac{v_- - v_o}{R} = -i_s \qquad v_- = v_o - i_s R$$

Now we introduce the VCVS constraint:

$$v_o = \mu(v_s - v_-)$$

Eliminating v_- between these two equations, we have:

$$v_o = \mu(v_s - v_-) = \mu(v_s - v_o + i_s R)$$

$$v_o = \frac{\mu(v_s + R i_s)}{1+\mu}$$

Also:

$$\begin{aligned} v_- &= v_o - i_s R \\ &= \frac{\mu(v_s + R i_s)}{1+\mu} - i_s R \\ &= \frac{\mu v_s - R i_s}{1+\mu} \end{aligned}$$

We now let $\mu \to \infty$:

$$v_o = v_s + R i_s$$

This equation is the solution.

We also have for $\mu \to \infty$:

$$v_- = v_s$$

But from the circuit diagram, we have:

$$v_+ = v_s$$

It therefore follows that:

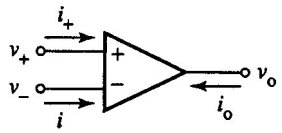
$$v_+ = v_-$$

In other words, the voltages at the op-amp input terminals are identical

Or we can say that the differential input voltage of the ideal op-amp is zero

Note that from the property of the VCVS, the op-amp input currents are also zero

To summarise, for the ideal op-amp:



The constraints imposed on the circuit to which it is connected are:

$$v_+ - v_- = 0 \qquad \text{and} \qquad i_+ = i_- = 0$$

The first equation is the same as that for a <u>short circuit</u> and the second is that for an <u>open-circuit</u>

This means that the two terminals act simultaneously like both a short-circuit and an open-circuit

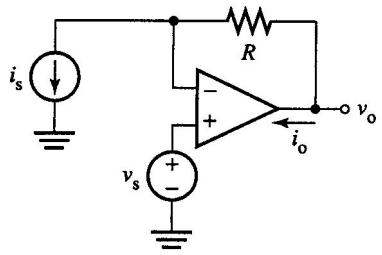
For this reason, it is often said that the two input terminals form a <u>virtual short-circuit</u>

The fact that the input voltage is zero explains how a device having infinite gain does not necessarily have a finite output voltage

Consider now the expression for the circuit output voltage:

$$v_o = v_s + Ri_s$$

It depends on the independent sources v_s and i_s and also on the passive element value R, but does not depend on the ideal op-amp itself.



The amplifier output current i_o depends on i_s and on the load connected

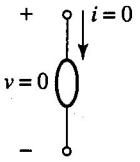
Thus the op-amp output terminal behaves such as to provide the output voltage and output current required by the rest of the circuit

The output terminal does not impose any constraint on its voltage or current but provides whatever is required by the rest of the circuit

In order to work with the constraints imposed by an ideal op-amp, it is helpful to introduce a special model called a nullor

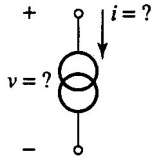
1.4 <u>Nullor Model for the Ideal Op-amp</u>

The virtual short-circuit with v = 0 and i = 0 that describes the op-amp input port may be represented by the following symbol:



This two-terminal element is called a nullator

The op-amp output port for which the voltage and current do not depend on the amplifier itself but on the surrounding circuit elements may be represented by the following symbol:



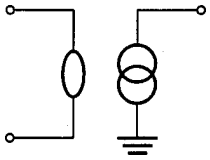
This two-terminal element is called a norator

The norator is a two-terminal element that does not have any effect whatsoever on the voltage across it or the current through it though it does provide a path for current to flow

By drawing the nullator and the norator symbols on a circuit diagram in place of the op-amp, we represent accurately the constraints imposed by the ideal op-amp

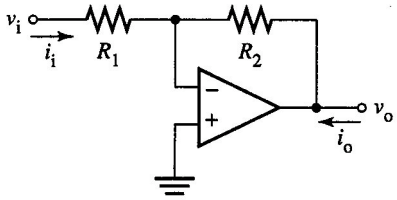
Because the nullator and the norator always occur in pairs in an op-amp circuit, we give the combination of these two elements: the name nullor

The infinite-gain VCVS at the output of an op-amp is grounded, so the nullor model for the op-amp has one terminal of the norator grounded as shown:



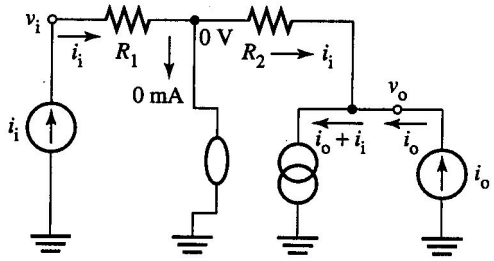
Example 11

Find a nullor equivalent for the op-amp sub-circuit shown:



Solution

We apply test sources and replace the op-amp by its nullor equivalent:



We note that the nullator holds the voltage at the middle node to zero

Furthermore, as the current into the nullator is zero, the current through R_2 is the same as that through R_1

Applying KCL at the middle node:

$$\frac{0-v_i}{R_1}+\frac{0-v_o}{R_2}=0$$

$$\frac{v_o}{v_i}=-\frac{R_2}{R_1}$$

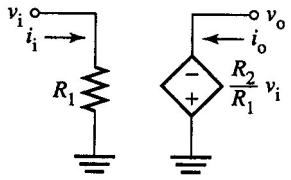
We can also write:

$$i_1=\frac{v_i-0}{R_1}=\frac{v_i}{R_1}$$

The second equation describes a resistance of value R_1 between the input terminal and ground

The first equation describes a VCVS from the output terminal to ground (v_o is independent of the current i_o and proportional to v_i

Thus, the equivalent sub-circuit is as shown:

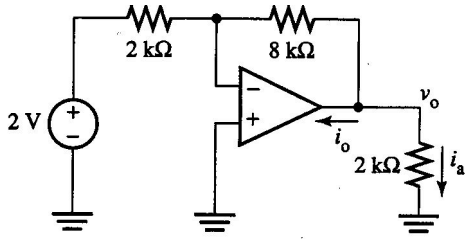


The practical importance of equivalent sub-circuits is that they allow one to design and analyze circuits rapidly by recognizing their topologies

Consider another example:

Example 5.12

Compute the voltage v_o, and currents i_a and i_o in the circuit shown:



Solution

We can quickly analyze this circuit for v_o by simply noting that this quantity is the negative of the ratio of the "feedback" resistor (8 kΩ) to the "input" resistor (2 kΩ) multiplied by the value of voltage at the input terminal (2 V)

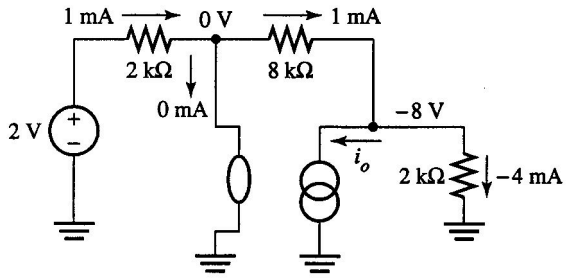
Thus, it is –8 V

We can then use Ohm's law to find that i_a = –8 V/2 kΩ = –4 mA

We can find i_o by observing that the top middle node is held to zero volt by the op-amp input terminals and that the current into the minus (or inverting) op-amp terminal is zero. This gives a current of 8 V/8 kΩ = 1 mA from left to right through the 8 kΩ resistor

KCL at the output node gives i_o = 1 mA – I_a = 1 mA – (– 4 mA) = 5 mA

The nullor equivalent circuit with the currents indicated is as follows:



If the 2 kΩ resistor at the output of the op-amp was changed to a 1 kΩ resistor, the op-amp output voltage (–8 V) would not change because it is governed by the voltage gain equation; therefore, the current in the load resistor would double to – 8 mA and the op-amp output current i_o would increase to 9 mA; this illustrates the fact that the op-amp output current does not have any constraint – it provides any current demanded by the rest of the circuit

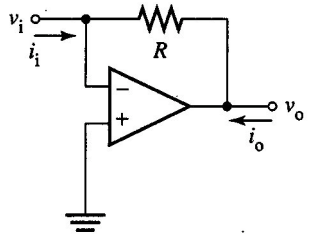
It is a fact that op-amps limit the current flowing in their output terminals, usually to a value of a few tens of mA

For this reason, a practical range of values for resistors in an op-amp circuit is on the order of a few hundred Ω to a few MΩ

Typical values are in the kΩ range, as we have seen

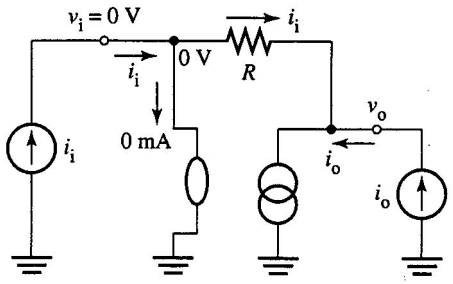
1.5 The Inverting Amplifier Topology

The sub-circuit shown below appears as part of a wide range of op-amp circuits encountered in practice:



Let's see what its characteristics are

We replace the op-amp symbol by its nullor equivalent and attach two test current sources (a voltage source would not work at the input because of the nullator constraint of zero voltage):



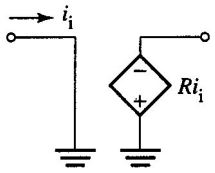
We see at once that $v_i = 0$ V, regardless of the value of the input current i_i

Because the current into the nullator is zero, the entire current i_i flows from left to right through the feedback resistor

Hence, we have $v_o = -Ri_i$ independent of the current i_o

This means that there is an equivalent CCVS between the output terminal and ground

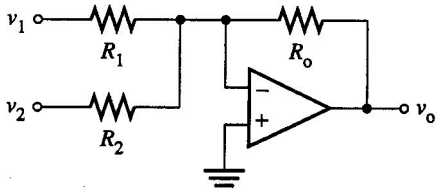
The complete equivalent sub-circuit is as follows:



Notice that resistor R has become the trans-resistance of the controlled source

Example 13

Find the voltage v_o for the circuit shown:



Solution

This circuit can easily be analyzed by applying KCL to the central node assuming a nullor model for the op-amp:

$$\frac{0-v_1}{R_1}+\frac{0-v_2}{R_2}+\frac{0-v_0}{R_0}=0$$

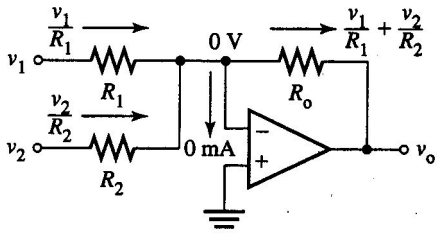
Hence:

$$v_0=-v_1\frac{R_0}{R_1}-v_2\frac{R_0}{R_2}$$

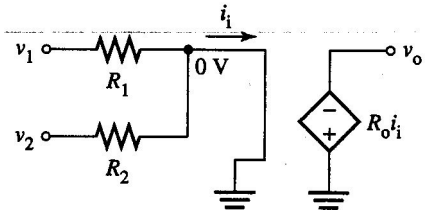
Thus, our circuit output is the weighted sum of the two input voltages

Clearly, we could add additional resistors to sum any number of additional input voltages

The currents flowing in the circuit are as follows:



We can solve the same example by using the CCVS equivalent for the op-amp and its feedback resistor R_o:



We can immediately see that the currents in the two input resistors add together to produce i_i and hence obtain the expression for v_0:

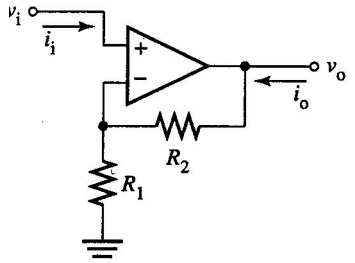
$$v_0=-R_0 i_i=-R_0\left(\frac{v_1}{R_1}+\frac{v_2}{R_2}\right)$$

1.6 The Basic Non-inverting Amplifier Topology

We now investigate another topology the non-inverting topology; in this case the input signal is fed to the + input terminal of the op-amp

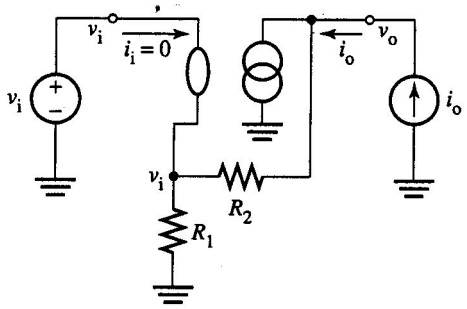
Example 14

Find an equivalent sub-circuit for the circuit shown:



Solution

We attach a test source at the input and one at the output and use the nullor model for the op-amp:



We have used a voltage source at the input because the input current is constrained to be zero by the nullator:

The nullator forces the voltage at the junction of the two feedback resistors to be the same as the input voltage v_i

We can apply KCL at this node:

$$\frac{v_i}{R_1} + \frac{v_i - v_o}{R_2} = 0$$

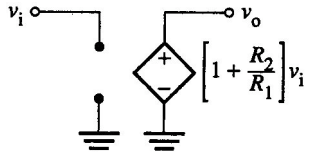
Hence:

$$v_0 = v_1\left(1 + \frac{R_2}{R_1}\right)$$

Because the input current of the whole circuit is zero independently of the input voltage, there is an equivalent open circuit between the input terminal and ground

The output voltage obeys the above equation independently of the output current i_o, so we see that there is an equivalent VCVS connected between the output terminal and ground

Thus, the equivalent circuit is as follows:



We see that it is non-inverting (the plus sign is at the top and the voltage gain is positive)

Unlike the inverting voltage amplifier, it presents an open circuit at the input; thus, it is exactly equivalent to an ideal voltage-controlled voltage source

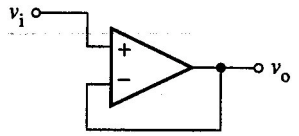
The voltage gain cannot be less than unity for the present configuration, whereas it can be less than unity for the inverting topology

1.7 The Voltage Follower (or Unity Gain Buffer)

If in the non-inverting amplifier circuit, we let $R_1 \rightarrow \infty$, we see that the voltage gain approaches unity, independently of R_2

Thus, we simply let $R_2 = 0$

This gives the following circuit:

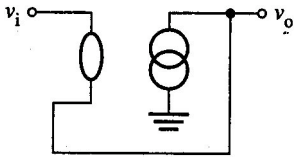


For this circuit:

$$v_o = v_i$$

This circuit is called a unity gain buffer or voltage follower

The nullor equivalent circuit is as follows:



Thus we can see that the input current is zero and the output current is provided by the norator at the amplifier output; the output current depends on the load connected

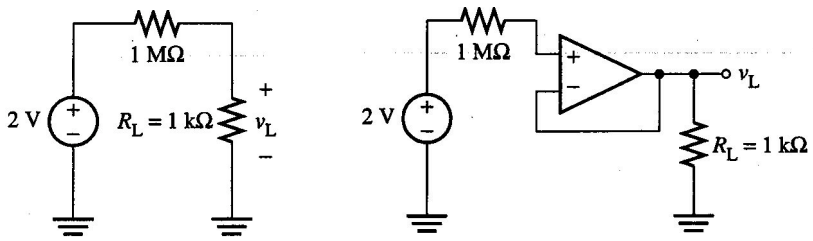
The voltage follower can therefore have substantial current gain

Although the voltage buffer does not provide any voltage gain, it is a useful configuration, as shown by the following example:

Example 15

A signal source with Thevenin equivalent voltage and resistance of 2 V and 1 MΩ has to be connected to a 1 kΩ load

Find the load voltage v_L and the power absorbed by the load resistor R_L for both circuit configurations shown:



Solution

For the circuit on the left, we use the voltage divider rule to obtain the voltage v_L:

$$v_L = \frac{1\ \text{k}\Omega}{1\ \text{M}\Omega + 1\ \text{k}\Omega} \times 2\ \text{V} = 0.002 = 2\ \ \text{mV}$$

The power absorbed by the load resistor is:

$$P_L = \frac{v_L^2}{1\ \text{k}\Omega} = \frac{4 \times 10^{-6}}{1 \times 10^3} = 4 \times 10^{-9} = 4\ \ \text{nW}$$

Now let's look at the circuit on the right above:

It is the same as the one on the left with the insertion of a unity gain buffer between the source elements and the load resistor R_L

The buffer presents an open circuit to the Thevenin equivalent of the source, so we see that the current through the 1 MΩ resistor is zero; thus, there is no voltage drop across it

Therefore, the voltage at the positive input terminal of the op-amp is the source value, 2 V

This same voltage is transferred to the load resistor; thus:

$$v_L = 2\ \ \text{V}$$

The power absorbed by the load resistor is:

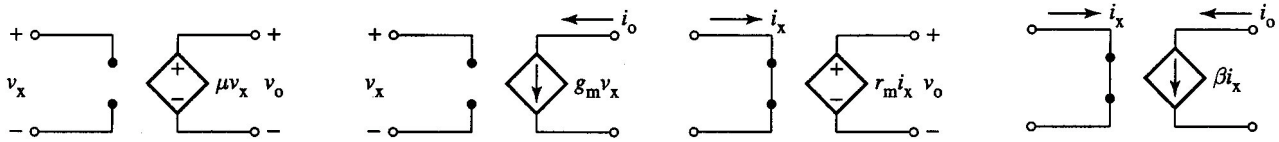
$$P_L = \frac{v_L^2}{1\ \text{k}\Omega} = \frac{4}{1 \times 10^3} = 4 \times 10^{-3} = 4\ \ \text{mW}$$

This is an increase in delivered voltage and power by factors of 1000 and 10^6, respectively

2 DERIVING THE NULLOR FROM DEPENDENT SOURCES

We have seen that the VCVS and the nullor are related; we now explore this relationship

Consider the four types of dependent source:



VCVS VCCS CCVS CCCS

We now let the gain of each type of dependent source tend to infinity, while assuming that the source voltage v_o and the source current i_o always remain finite

Then we can write:

$$\text{VCVS: } v_o = \mu v_x \qquad \therefore v_x = \frac{v_o}{\mu} \to 0 \quad \text{for} \quad \mu \to \infty$$

$$\text{VCCS: } i_o = g_m v_x \qquad \therefore v_x = \frac{i_o}{g_m} \to 0 \quad \text{for} \quad g_m \to \infty$$

$$\text{CCVS: } v_o = r_m i_x \qquad \therefore i_x = \frac{v_o}{r_m} \to 0 \quad \text{for} \quad r_m \to \infty$$

$$\text{CCCS: } i_o = \beta i_x \qquad \therefore i_x = \frac{i_o}{\beta} \to 0 \quad \text{for} \quad \beta \to \infty$$

Hence, we see that, for the voltage-controlled devices (VCVS and VCCS), their infinite gain forces their input voltage to zero

However, voltage-controlled devices (VCVS and VCCS) always behave like an open-circuit at their input irrespective of their gain, and hence their input current is always zero

Hence, for these voltage-controlled sources with infinite gain, both the input voltage and the input current are zero

It is also shown above that for the current-controlled devices (CCVS and CCCS), their infinite gain forces their input current to zero

But current-controlled devices (CCVS and CCCS) always behave like a short-circuit at their input and hence their input voltage is always zero

Hence, for these current-controlled sources with infinite gain, both the input voltage and the input current are zero

Thus, for all four controlled sources, both the input voltage and the input current are zero

Hence the input terminals of all four controlled sources behave like a nullator

Consider now the output terminals of the four controlled sources

We can now write:

$$\begin{aligned}
&\text{VCVS: } v_o = \mu v_x \;\rightarrow \infty \times 0 = \text{arbitrary for } \mu \rightarrow \infty \\
&\text{VCCS: } i_o = g_m v_x \rightarrow \infty \times 0 = \text{arbitrary for } g_\text{m} \rightarrow \infty \\
&\text{CCVS: } v_o = r_m i_x \;\rightarrow \infty \times 0 = \text{arbitrary for } r_\text{m} \rightarrow \infty \\
&\text{CCCS: } i_o = \beta i_x \;\;\rightarrow \infty \times 0 = \text{arbitrary for } \beta \rightarrow \infty
\end{aligned}$$

In the limit as the gain parameters becomes infinite and the input variable becomes zero, the output variable in each case becomes arbitrary (or indeterminate)

We see that, for the controlled voltage sources (VCVS and CCVS) with infinite gain, the output voltage becomes arbitrary

However, for voltage sources of any gain the output current is always arbitrary

Hence, for these sources, both output voltage and output current are arbitrary

It is also seen that for the controlled current sources (VCCS and CCCS) with infinite gain, the output current becomes arbitrary

However, for current sources of any gain the output voltage is always arbitrary

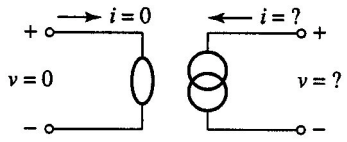
Hence, for these sources too, both output voltage and output current are arbitrary

Hence, for all four sources with infinite gain, the output voltage and output current are arbitrary

In other words they place no constraints on their output voltage nor on their output current; output voltage and output current are determined by other elements in the circuit

It follows that the output terminals of all four controlled sources behave like a norator

Hence, we have shown that each of the dependent sources when their gain is infinite is equivalent to the nullor:



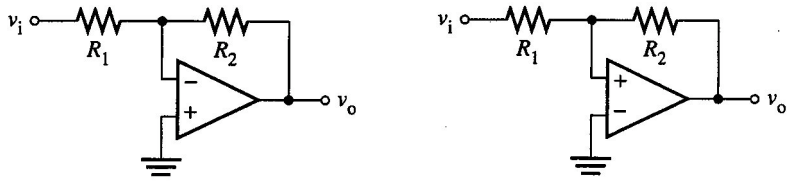
Note that, if the nullor were the model of an op-amp, then the norator is grounded

3 SOME PRACTICAL ASPECTS OF OP-AMPS; STABILITY AND FEEDBACK

3.1 Introduction

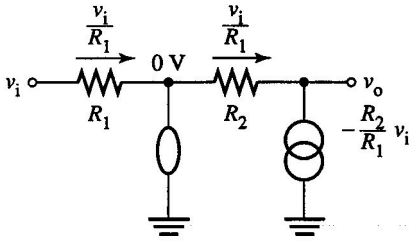
In all circuits studied so far, there was a "feedback resistor" connected between the output of the op-amp and the negative input terminal; this is no coincidence, as we shall now show

Consider the two sub-circuits shown:



The only difference between the two is the feedback resistor R_2: it is returned to the negative op-amp input in one and to the positive input in the other

If the op-amp is ideal in both circuits then both are equivalent to the same nullor equivalent circuit shown:



Hence, with an ideal op-amp the circuits should behave the same

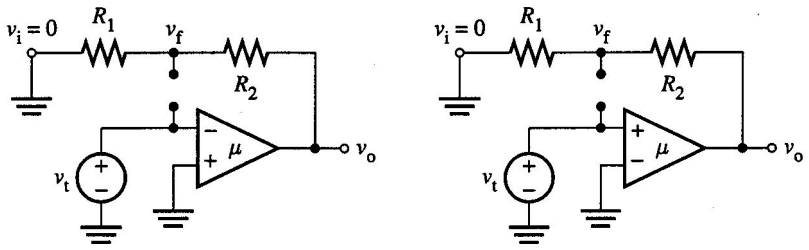
However, no real circuit behaves in an ideal fashion

In practice, the two circuits behave quite differently; the main difference is their stability properties

In order to investigate stability of a circuit, we de-activate all independent sources, in this case the input voltage source v_i

Each circuit has a feedback loop, going from an op-amp input terminal, through to the output terminal of the op-amp, then through the resistor R_2 and then back to the same op-amp input terminal

In order to explore circuit stability, we cut the feedback loop and insert a test source in order to determine the loop gain; we now make the cut in the lead feeding into the input terminal of the op-amp:



The test signal v_t is amplified by the amplifier, and comes back through R_2 to its starting point where we label the voltage v_f (for feedback voltage):

We represent the op-amp by a VCVS having a finite voltage gain μ

Performing this procedure for the circuit on the left and on the right, we have:

$$v_{f(left)} = -\frac{\mu R_1}{R_1 + R_2} v_t = -\mu F v_t \qquad v_{f(right)} = +\frac{\mu R_1}{R_1 + R_2} v_t = +\mu F v_t$$

F is the voltage division ratio which determines v_f from v_o; F is called the feedback factor:

$$F = \frac{R_1}{R_1 + R_2}$$

We define the loop gain by the equation:

$$LG = \frac{v_f}{v_t}$$

We see that the circuit on the left above has loop gain:

$$LG_{(left)} = -\frac{\mu R_1}{R_1 + R_2} = -\mu F \qquad LG_{(right)} = +\frac{\mu R_1}{R_1 + R_2} = +\mu F$$

We say that the circuit has positive feedback if LG > 0 and negative feedback if LG < 0

Since F and μ are positive, the left circuit has negative feedback and the right circuit has positive feedback

3.2 Negative and positive feedback

In order to determine the effects of positive and negative feedback, consider that we re-join-up the circuit where we broke it and remove the test source v_t at the same time, but we remember that the loop gain is negative and positive for the left and right circuits respectively

Since there is no independent source, we can assume that all voltages and currents are zero

We then assume that there is a source of interference, perhaps a mobile phone transmitting, and that the signal is picked up by the wire connected to the op-amp input terminal

In the case where there is positive feedback, the interfering signal will be amplified as it traverses the loop and will appear instantaneously at the point where the interference was picked up considerable amplified and in phase with the interference signal; this amplified signal will in turn be amplified again; the result is that the voltages in the circuit will increase uncontrollably until they are limited by the power supply voltage of ±5 V or ±15 V; the circuit will cease to operate correctly as an amplifier of the input signal

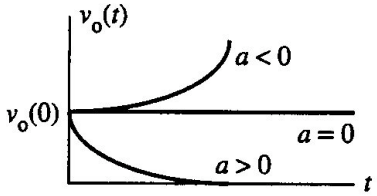
Consider now the case where there is negative feedback; the situation will be similar up to the point where the amplified interference signal appears again at the op-amp input, but in this case the amplified signal is 180^0 out of phase with the interfering signal and will therefore tend to cancel the effect of the interfering signal

The negative feedback case requires some assumptions about the dynamics of the op-amp for a precise analysis, but it may be shown that with negative feedback, following a burst of interference, all voltages and currents will tend towards their DC steady state values of 0 V and 0 A; in other words the circuit is stable

Depending on the dynamics of the op-amp, output voltage versus time for a stable and unstable circuit could have typical forms:

$$v_o(t)_{(stable)} = Ae^{-t/\tau} \qquad v_o(t)_{(unstable)} = Ae^{+t/\tau}$$

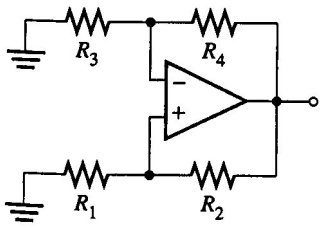
The corresponding waveforms are as follows:



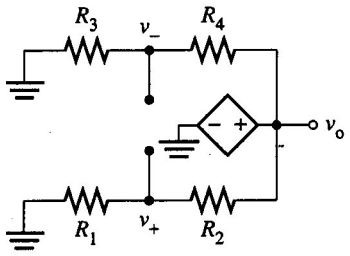
So far, we have considered a circuit which may have either negative or positive feedback

In practice, circuits often have elements connected to both input terminals, which means that both positive and negative feedback is occurring

Such cases can be represented by a generic op-amp circuit:



For this circuit, we split the feedback loop as follows:



Then we define different feedback factors for the + and – input terminals of the op-amp:

$$F_+ = \frac{R_1}{R_1 + R_2} \qquad F_- = \frac{R_3}{R_3 + R_4}$$

where:

$$v_+ = F_+ v_o \qquad v_- = F_- v_o$$

The condition for a circuit to be stable is:

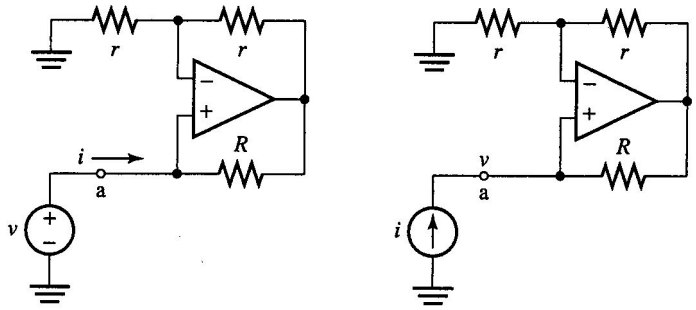
$$F_- > F_+$$

If $F_- < F_+$, the circuit is unstable

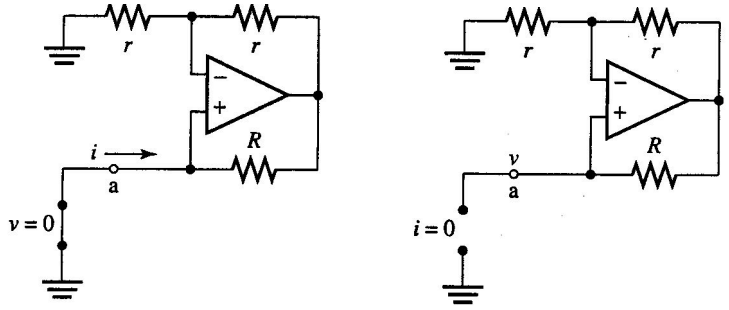
If $F_- = F_+$, we say that the circuit is on the borderline between stability and instability (or marginally stable/unstable)

3.3 Example of Stability Testing

We show a circuit which realises negative resistance being tested by a v-source and by an i-source



To test the stability, we consider an equivalent circuit with sources deactivated:



For the voltage driven circuit on the left, we have:

$$F_+ = 0 \qquad F_- = 0.5$$

Since $F_- > F_+$, the circuit is <u>stable</u>

For the current driven circuit on the right:

$$F_+ = 1 \qquad F_- = 0.5$$

Since $F_+ > F_-$, the circuit is <u>unstable</u>

Notice that stability can be different when a circuit is driven by a voltage source and by a current source

This example circuit is said to be short-circuit stable and open-circuit unstable

This analysis shows that the source forms an important part of the circuit when determining stability

When op-amp feedback circuits contain inductors and capacitors as well as resistors, and when op-amp models have finite bandwidth and therefore time constants, then the feedback factors have phase as well as magnitude

In that case, the approach has to be more general than in this simple preliminary study

4 NODAL ANALYSIS OF CIRCUITS WITH OP-AMPS

4.1 <u>General approach</u>

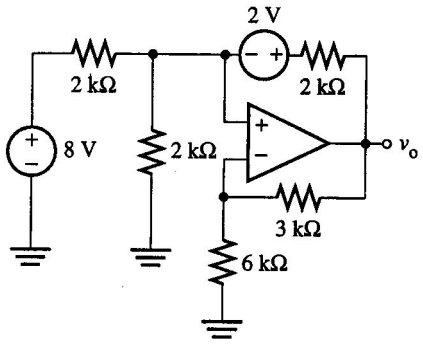
For analysis, an ideal op-amp can be replaced with any of the four types of dependent sources, provided that the gain parameter is allowed to become infinite

Thus, when we are carrying out nodal analysis, we can choose any of the four dependent sources as a model

Voltage constraints are easier to work with in nodal analysis, so we will choose a voltage-controlled model

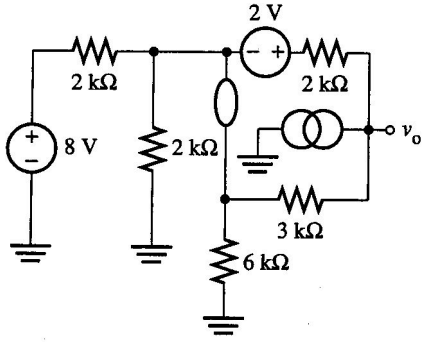
Because each voltage source reduces the number of nodal equations by one, we will choose it to be a voltage-controlled voltage source (VCVS)

Consider an example circuit containing an op-amp:

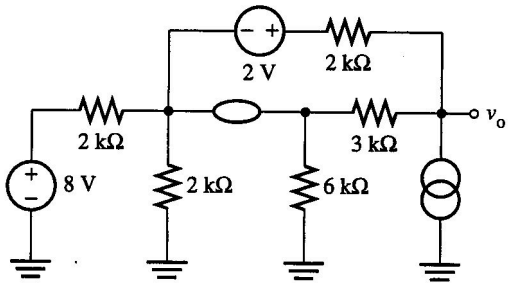


First we check stability of the circuit: we deactivate both voltage sources and compute the positive and negative feedback factors F_+ and F_-; these turn out to be $F_+ = 1/3$ and $F_- = 2/3$; hence the circuit is stable

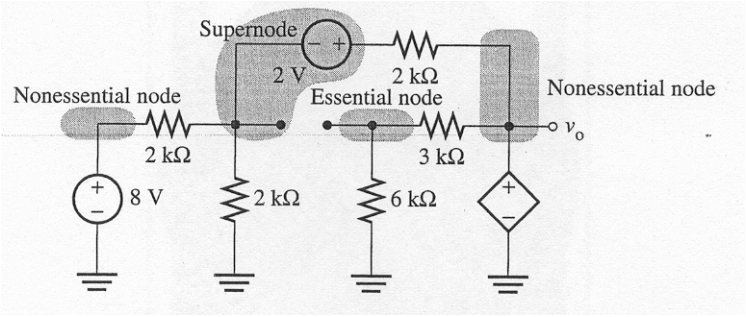
Our first step in the analysis using the nodal method is to replace the op-amp by its (grounded) nullor equivalent:



It is sometimes helpful to alter the circuit layout slightly to an equivalent form with a ladder structure:



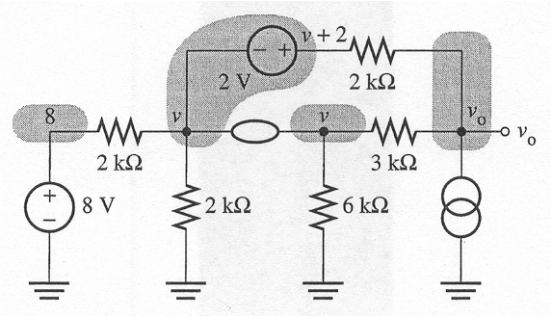
Now we temporarily replace the nullor with its VCVS equivalent:



We see there are two non-essential nodes, one super-node, and one essential node; thus, we anticipate two KCL equations

Note that the dependent source is treated like an independent source when determining non-essential nodes

Returning to our nullor version of the circuit, we prepare it for nodal analysis as shown:



We must write one equation at the super-node and one at the essential node

However, the voltages on either side of a nullator are the same and this means that the super-node and the essential node have the same voltage, which we label as v

Although their voltages are the same, we apply KCL to each node separately, remembering that the nullator carries zero current

$$\frac{v-8}{2}+\frac{v}{2}+\frac{v+2-v_o}{2}=0 \quad \text{(for supernode)}$$

$$\frac{v}{6}+\frac{v-v_o}{3}=0 \quad \text{(for essential node)}$$

Note that we have used the self-consistent units of kΩ, mA, and V

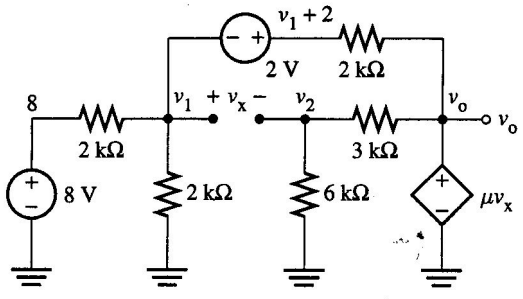
We can easily solve the KCL equations to get v = 4 V and v_o = 6 V

The solution can easily be checked by looking at the circuit

To establish confidence, we now repeat the above analysis using a VCVS with finite gain, and then let the VCVS gain go to infinity in order to represent the ideal op-amp

4.2 Justification for the Nullor Model

The version of the circuit with the op-amp replaced by a finite gain VCVS is as follows:



where now node voltages v_1 and v_2 in general have different values

The nodal equations at the super and essential nodes are:

$$\frac{v_1-8}{2}+\frac{v_1}{2}+\frac{v_1+2-v_o}{2}=0 \quad \text{(for supernode)}$$

$$\frac{v_2}{6}+\frac{v_2-v_o}{3}=0 \quad \text{(for essential node)}$$

Untaping the VCVS we can write:

$$v_o = \mu(v_1 - v_2)$$

Using this equation to eliminate v_o in the above equations, we have the matrix equation:

$$\begin{bmatrix} 3-\mu & \mu \\ -2\mu & 3+2\mu \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 6 \\ 0 \end{bmatrix}$$

Solving, we have:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} \dfrac{2(3+2\mu)}{3+\mu} \\ \dfrac{4\mu}{3+\mu} \end{bmatrix}$$

Consequently, we can write:

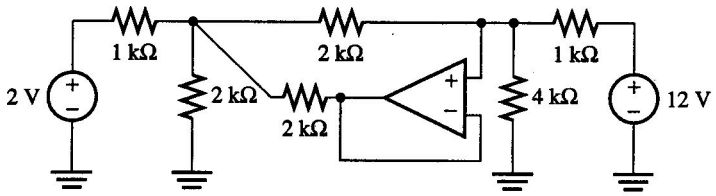
$$v_o = \mu(v_1 - v_2) = \frac{6\mu}{3+\mu}$$

Computing the limit as $\mu \to \infty$, we see that $v_1 = v_2 = 4$ V and $v_o = 6$ V, as before

It may be shown that repeating the analysis with the op-amp replaced by any of the four types of controlled source with a finite gain and letting gain $\to \infty$ leads to the same result

Example16

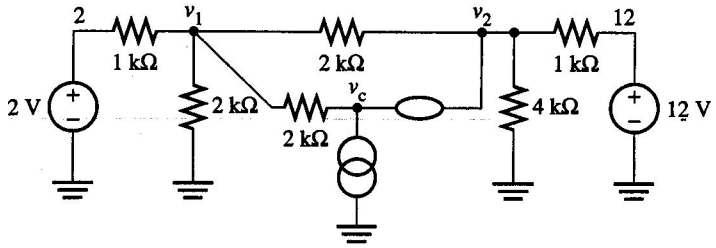
Solve the circuit below using nodal analysis:



Solution

The feedback factors are $F_- = 1$ and $F_+ = 1/14$; hence this op-amp circuit is stable

We apply nodal analysis using a nullor to replace the buffer:



We have labelled the node at the top of the norator with the symbol v_c, for we are considering it (from a topological point of view) to be a VCVS (with gain $\to \infty$)

Note that due to the norator, node v_c is a non-essential node

The KCL equations at the two essential nodes v_1 and v_2 are, therefore:

$$\frac{v_1 - 2}{1} + \frac{v_1}{2} + \frac{v_1 - v_2}{2} + \frac{v_1 - v_c}{2} = 0 \quad \text{(for node } v_1\text{)}$$

$$\frac{v_2}{4} + \frac{v_2 - 12}{1} + \frac{v_2 - v_1}{2} = 0 \quad \text{(for node } v_2\text{)}$$

Putting $v_c = v_2$ and solving, we have:

$$\begin{bmatrix} \frac{5}{2} & -1 \\ -\frac{1}{2} & \frac{7}{4} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 2 \\ 12 \end{bmatrix}$$

The solution to this equation is: $v_1 = 4$ V and $v_2 = 8$ V

5 TRANSISTOR CIRCUITS

5.1 Introduction

The transistor is certainly a very important circuit component because it is used to construct all the key building blocks of digital and analogue circuits from logic gates to operational amplifiers

It is also an important component in its own right for analogue circuit design both in integrated circuits and non-integrated circuits

Transistors are of two main types:

The bipolar junction transistor (BJT) was invented in 1947 and was the main active device until about 1970

The field effect transistor (FET) became important in about 1970 in the form of CMOS-FETs (complementary metal-oxide-semiconductor - FETs) and rapidly took over from the BJT for most digital and analogue applications

The reasons for the success of CMOS-FETs is their low power consumption, ease of design and their small size which allows the development of very large scale integrated (VLSI) circuits with over 10^6 transistors on a single chip

Transistors in most applications need to be operated with power supplies; these are usually DC voltage sources or DC current sources; application of suitable DC sources to a transistor to allow it to operate is called biasing and the components that do this constitute the bias circuit

Transistors are active devices which are able to amplify a small input signal to produce a larger output signal

A small AC input signal can effectively modulate the DC power supplied to the transistor from its biasing circuits so that some of the modulated DC power appears as a transistor AC output signal

This means that the input and output signals of a transistor consist of both DC (bias) and AC (signal) components superimposed

In many applications, it is important that the relationship between the AC input signal and the AC output signal is linear; for instance to avoid distortion in an audio application

It is thus common practice to separate the linear AC operation of the transistor and produce a linear AC equivalent circuit which describes this important aspect of behaviour

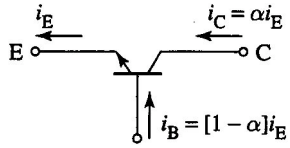
In this section we will look at some linear AC equivalent circuits for transistors and apply the methods of circuit analysis to determine AC responses for given AC input signals

The term 2 course ‘Analogue Electronics’ will provide a detailed study of different types of transistors, the design of suitable biasing circuits and the extraction of linear AC equivalent circuit models of the type we use here

We emphasise again that the transistor circuits we give here will not work as given because power supplies are not included at this stage; this material is presented to provide familiarity in working with linear AC equivalent circuits for transistors which will be used extensively in later courses

5.2 The Bipolar Junction Transistor (BJT): Basic Operation

The circuit symbol for the bipolar junction transistor (BJT) is depicted below:



The three terminals are labelled E for emitter, B for base, and C for collector

BJTs are of two types called NPN and PNP depending on their construction; in the symbol for an NPN transistor, the arrow on the emitter points from the base and towards the emitter (as above); in the symbol for a PNP transistor, the arrow on the emitter has the reverse orientation

The operation of the transistor can be explained briefly as follows:

Consider an external current i_E in the form of electrons to be injected into the device from the emitter

99 % of the electrons that are injected go across the base region and emerge from the collector terminal; this fraction of electrons is denoted α; thus the collector current is αi_E

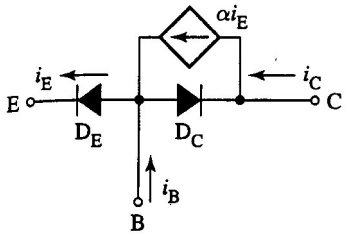
However, 1 % of the electrons that are injected at the emitter undergo a process called recombination which leads to base current $(1-\alpha)i_E$ which is much smaller than i_E and i_C

In reality, the base current would be the input signal and emitter current i_E or collector current i_C would be the output signal, an output signal about 100 times as large as the input base current

Recalling that electron motion to the right constitutes conventional current to the left, we see that the three terminal currents have the directions shown in the diagram above

5.3 BJT Models

We are now in a position to form a model for a BJT:



It consists of two diodes and a current-controlled current source (CCCS)

The current source imposes the required relationships between the terminal currents:

$$i_C = \alpha i_E$$
$$i_B = (1-\alpha) i_E$$

In all the working so far, currents have been represented using lower-case 'i' and upper-case E, B and C. By convention, this implies that the currents are total instantaneous currents, that is they consist of the DC components due to the bias circuits plus the AC components due to the signal

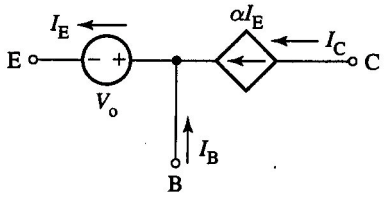
We now split the model for total instantaneous currents into separate DC and AC models

The diode will be covered in the Analogue Electronics course. Here, we simple state that the diode has a voltage drop of around +0.7 V when current is flowing in the forward direction (in line with the arrow in its symbol) and is approximately equivalent to an open-circuit (hence zero current) when the applied voltage is in the reverse direction

An NPN transistor is biased so that the collector is at a more positive voltage than the base and therefore the diode D_C is reverse biased and may be ignored

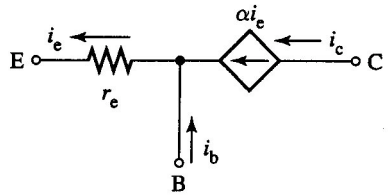
The diode D_E is forward biased and therefore the transistor base voltage tends to be about +0.7 V with respect to the emitter voltage

Hence for the DC model, we can replace D_E by a 0.7 V voltage source V_0:



Note that this DC model can not predict AC signals correctly; it is useful however for design of bias circuits. In the DC model, currents are represented by upper-case I and upper-case E, B and C

For the AC small signal model (which will be derived properly in the Analogue Electronics course), we can replace D_E by a resistor r_e that depends upon the DC value of emitter current:

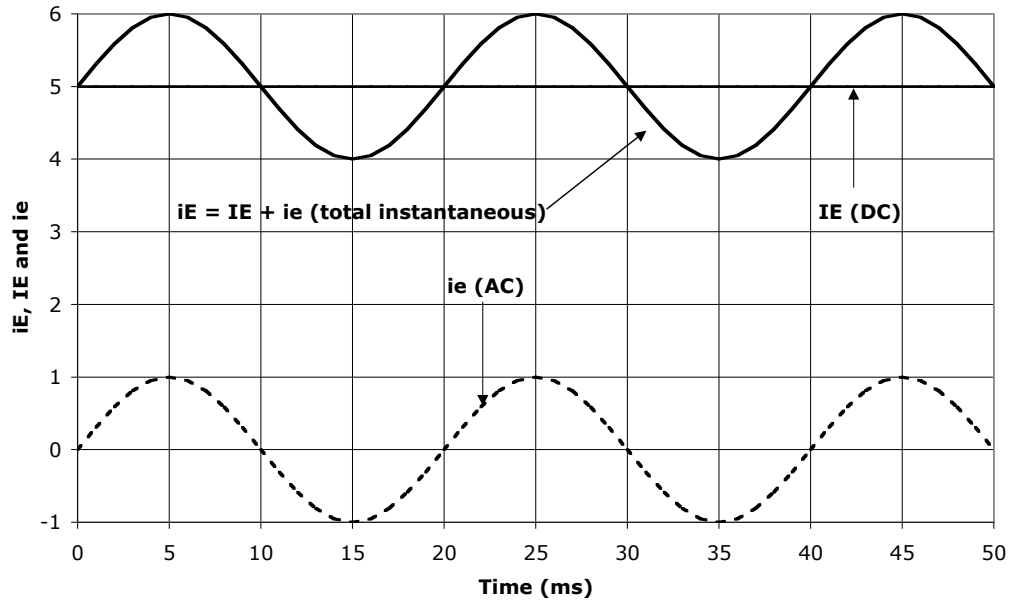


Note that this AC model cannot predict DC signals correctly; for instance, the fact that the base voltage is around 0.7 V higher than the emitter is no longer apparent. In the AC model, currents are represented by lower-case i and lower-case e, b and c

It may be shown that the r_e is given by:

$$r_e = \frac{V_T}{i_E} \quad \text{where} \quad V_T = 25 \text{ mV}$$

where i_E is the total instantaneous emitter current. Since this current consists of a DC bias value I_E with an AC signal component i_e superimposed then, strictly, r_e will vary with the AC signal waveform variations



The analysis can be simplified considerably if we perform a small-signal AC analysis

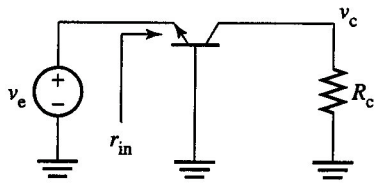
In this approach, we assume that the amplitude of the AC part of the signal i_e is sufficiently small compared with the DC value I_E that the variations in r_e are negligible and it can be assumed to be constant governed by the bias or DC value I_E

This effectively means that we can treat the circuit as linear even though it is strictly non-linear

From now on, we concentrate upon the AC small signal model and its analysis

Example 20

Find the small signal input resistance $r_{in} = v_e/i_{in}$ and voltage gain $A_v = v_c/v_e$ of the BJT circuit shown:

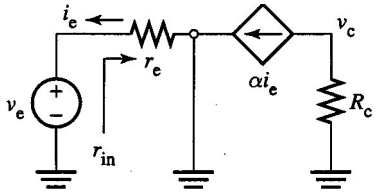


Notes:

1) This is a small signal AC equivalent circuit; the DC sources have already been de-activated for the analysis and are not shown
2) In this circuit, we say that the transistor is in common base configuration since the base terminal is the reference node for both the input and output voltages of the transistor
3) Input resistance is the resistance presented to the input voltage source by the amplifier
4) Voltage gain is the ratio of the output (collector) voltage v_c to the input (emitter) voltage v_e

Solution

We first replace the transistor symbol by its small signal equivalent circuit:



Note that we use an upper-case R to denote circuit elements and lower case r to denote component within elements models

There is only one essential node, the output terminal (collector terminal of the BJT) – so only one KCL nodal equation is required:

$$\frac{v_c}{R_c} + \alpha i_e = 0$$

The controlling variable i_e for the CCCS can be expressed in terms of the input source voltage v_e:

$$i_e = -\frac{v_e}{r_e}$$

Hence:

$$v_c = \frac{\alpha R_c}{r_e} v_e$$

Thus, the small signal voltage gain is:

$$A_v = \frac{v_c}{v_e} = \frac{\alpha R_c}{r_e}$$

The A stands for amplification and the v refers to the fact that it is voltage that is being amplified

The current gain ($A_i = i_c/i_e$) is equal to $\alpha \cong 0.99$

Finally, the input resistance of the circuit is given by:

$$r_{in} = \frac{v_e}{-i_e} = r_e$$

Let's get some idea of practical values

We assume that the transistor is biased by a biasing circuit (not shown) such that the DC value of emitter current I_E is 1 mA

Then we can immediately compute:

$$r_{in} = r_e = \frac{V_T}{I_E} = \frac{0.025}{0.001} = 25 \ \ \Omega$$

and:

$$A_v = \frac{v_c}{v_e} = \frac{\alpha R_c}{r_e} \approx \frac{R_c}{r_e} \approx \frac{5000}{25} \approx 200$$

Thus, the collector voltage is much larger: than the emitter voltage

Notice that the input source establishes a current i_e in the low-valued emitter diode resistance r_e, and the BJT reproduces that same current in the much larger resistance R_c through the action of the CCCS

It is from this principle that the name transistor comes: transferring current through a resistor

Though the voltage gain of the common base circuit is large, the input resistance is small

Thus, if the Thevenin resistance of the input source is non-zero, a sizable voltage drop will occur at the input, and the overall voltage gain will be reduced

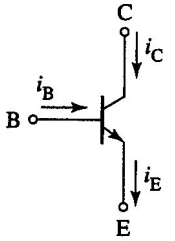
This is a disadvantage of the configuration

Another is the fact that the current gain is less than unity

The common-emitter configuration overcomes these limitations

5.4 The Common Emitter Small Signal Model for the BJT

Suppose we twist the BIT around so that the base terminal is the input terminal:



Since the base current is given by $(1 - \alpha)i_E$ and $\alpha \cong 0.99$, then the input current i_B is very small

We would therefore expect that both the current gain and the input resistance would be much higher than for the common base circuit

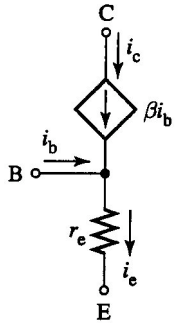
It is helpful to define a new parameter β which is the current gain in common-emitter configuration:

$$\beta = \frac{i_C}{i_B} = \frac{\alpha i_E}{(1-\alpha) i_E} = \frac{\alpha}{1-\alpha}$$

Thus for a typical value for α of 0.99, then β will be 0.99/(1 – 0.99) = 99

We have been working with total instantaneous variables, but the same relationship holds, of course, for small signal ones

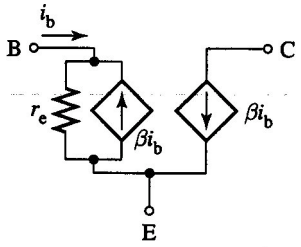
Expressing the CCCS current expression in terms of β, we have the small signal equivalent circuit shown:



5.5 The Small Signal Hybrid–π Model for the BJT

Since in common-emitter configuration the emitter of the transistor is usually grounded, analysis is easier if the controlled current source is connected to the emitter rather than to the base terminal

We can replace the single current source between collector and base by two current sources of same current value where one is connected from collector to emitter and one from emitter to collector:



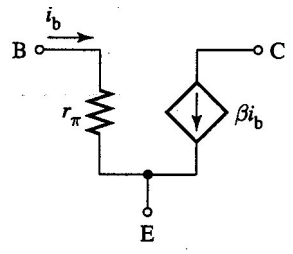
The current through r_e is $i_b + \beta i_b = i_b(1 + \beta)$; hence the voltage between the B and E terminals is:

$$v_{be} = r_e i_b (1+\beta)$$

Since the current flowing between the b and e terminals is i_b, it follows that there is an equivalent resistance between the B and E terminals of:

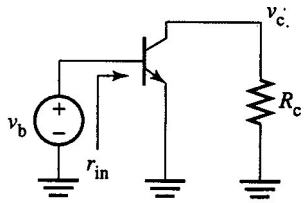
$$r_\pi = \frac{v_{be}}{i_b} = r_e(1+\beta)$$

This leads to the hybrid-π model for the transistor:



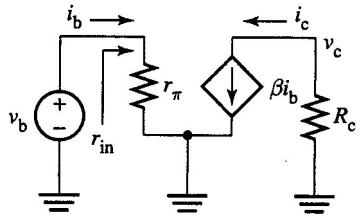
Example 21

Find the small signal voltage gain $A_v = v_c/v_b$ and the small signal input resistance of the common emitter voltage amplifier whose small signal equivalent circuit is shown:



Solution

Just as for the common base circuit, we replace the BJT symbol with its small signal equivalent circuit, in this case the hybrid–π model:



There is only one essential node the collector terminal of the BJT

The nodal equation is:

$$\frac{v_c}{R_c} + \beta i_b = 0$$

We now express the controlling variable for the controlled source i_b in terms of the independent source variable v_b:

$$i_b = \frac{v_b}{r_\pi}$$

These two equations give the voltage gain:

$$A_v = \frac{v_c}{v_b} = \frac{-\beta i_b R_c}{i_b r_\pi} = -\frac{\beta R_c}{r_\pi}$$

Substitution of the expression for r_π in terms of r_e shows that the voltage gain is the same as that for the common base amplifier apart from the minus sign:

$$A_v = -\frac{\beta R_c}{r_\pi} = -\frac{\beta R_c}{r_e(1+\beta)} = -\frac{\alpha R_c}{r_e}$$

Note that $\beta = \dfrac{\alpha}{1-\alpha}$ reverses to $\alpha = \dfrac{\beta}{1+\beta}$

The minus sign in the voltage gain expression for the common-emitter amplifier implies that there is a 180^o phase shift between the output and input signals

However, the input resistance of the common emitter amplifier r_π is $(\beta + 1)$ times as large as the value for the common base circuit r_e

The current gain is clearly equal to β, a factor of $\beta + 1$ times as large as for the common base circuit since $\beta/\alpha = 1/(1 - \alpha) = \beta + 1$

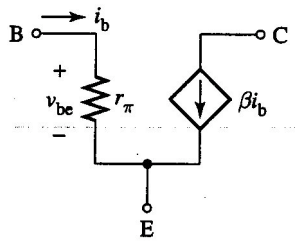
Thus, the common emitter circuit has the same voltage gain magnitude, a higher current gain, and a higher input resistance

These factors lead to the highest power gain that can be produced by a transistor and an amplifier circuit which can be readily cascaded to lead to enormously high overall gains, as required, for instance, in a radio receiver

5.6 The Ideal BJT Model

For an ideal BJT, the CCCS in its model would have an infinite β just as an ideal op-amp is equivalent to a VCVS with infinite voltage gain

Let's get some idea of how to treat such a case by looking more closely at the hybrid–π model:



Let's convert the controlling variable for the controlled source from i_b to v_{be}

This gives the CCCS constraint equation:

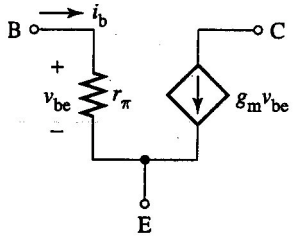
$$\beta i_b = \beta \frac{v_{be}}{r_\pi} = \frac{\beta}{r_\pi} v_{be} = \frac{\beta}{(\beta+1)r_e} v_{be} = \frac{\alpha}{r_e} v_{be} = g_m v_{be}$$

where

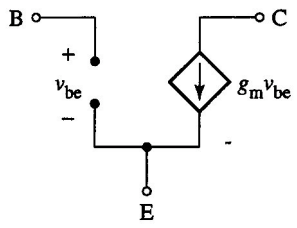
$$g_m = \frac{\beta}{r_\pi} = \frac{\alpha}{r_e} \approx \frac{1}{r_e}$$

is called the transconductance which depends on r_e and is practically independent of β

The resulting hybrid–π model with a VCCS is as follows:



If we let $\beta \to \infty$, then $r_\pi \to \infty$ and we have the following equivalent circuit:



Notice that the transconductance has the unit Siemens (inverse Ω)

The subscript m stands for mutual which means that the current in one pair of terminals has something mutual (in common) with the voltage between another pair

It is synonymous with the trans- in transconductance

The hybrid–π model in terms of g_m we have derived is a good model for describing field-effect-transistors (FETs) and is immensely important for this reason

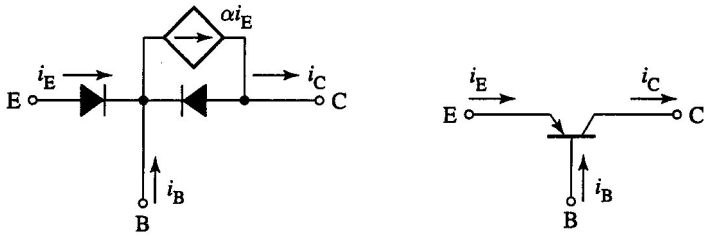
Note that if the BJT becomes fully ideal then we have $g_m \to \infty$; under this condition, the BJT (or FET) may be replaced by a nullor as was done for the ideal op-amp

However, the gap between practical transistor behaviour and ideal behaviour predicted using a nullor equivalent is much greater than in the case of op-amps

5.7 The PNP BJT

BJTs occur in two forms, the NPN device we have been considering and the PNP device

The model and symbol for the PNP BJT are as follows:



We see that the directions of all total instantaneous currents are reversed compared with the NPN transistor

This means that all bias voltages and currents are the negative of those for an NPN transistor

However, it does not affect the small signal AC operation and the small signal AC model is identical to that for the NPN BJT

Thus the same small signal AC models may be used for NPN and PNP transistors

6 FREQUENCY RESPONSE OF OP-AMP AND TRANSISTOR CIRCUITS

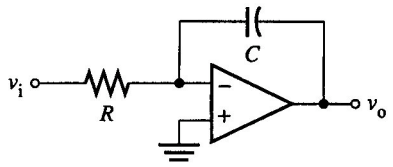
6.1 General

We have developed op-amp and transistor circuits with the resistor as the sole passive element. We now introduce the capacitor and the inductor to these circuits. Then, we will look at the intrinsic frequency response of the op-amp itself. We begin by considering examples of circuits containing op-amps, resistors and capacitors, namely active-RC circuits.

6.2 Inverting op-amp topology

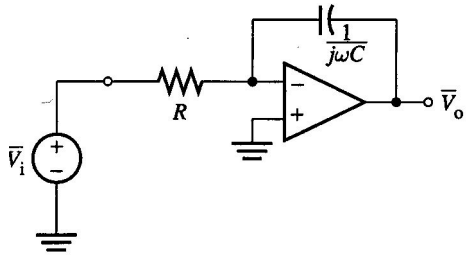
We begin by considering an example

Example 14: Determine the voltage gain function v_o/v_i and sketch the Bode gain plot for the circuit shown assuming that the op-amp is ideal:



Solution

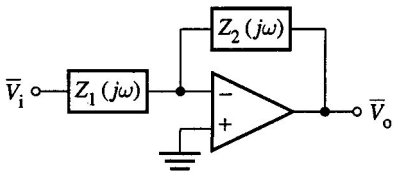
We first add a sinusoidal test source at the general frequency ω and draw the phasor equivalent circuit:



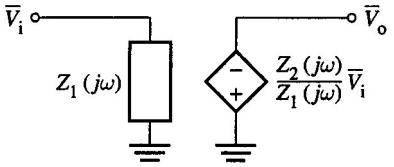
A number of analysis approaches are possible: we could replace the op-amp by its nullor equivalent and perform nodal analysis

However, our approach is to make use of the general equivalent for the op-amp inverting configuration which we derived assuming resistors

We now replace the resistors by general impedances:



The equivalent circuit we derived previously with resistors replaced by impedances is as follows:



We now let:

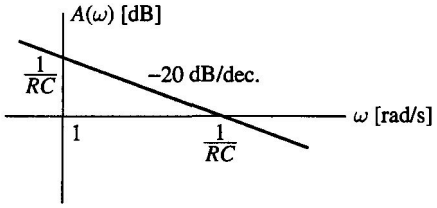
$$Z_1(j\omega) = R \qquad Z_2(j\omega) = \frac{1}{j\omega C}$$

Hence, the voltage gain is:

$$\frac{\overline{V_o}}{\overline{V_i}} = H(j\omega) = -\frac{Z_2(j\omega)}{Z_1(j\omega)} = -\frac{1/j\omega C}{R} = -\frac{1}{j\omega CR} = j\frac{1}{\omega CR} = \frac{1}{\omega CR}\angle 90^\circ$$

The phase is constant (at 90°) with respect to frequency, so we do not need to plot it

The gain plot is a straight line with a slope of –20 dB/decade:



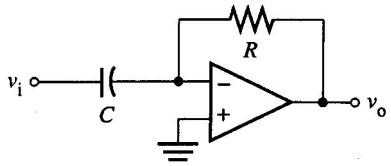
This circuit is referred to as an integrator circuit; it may be shown that the output voltage is the integral of the input voltage

$$v_o(t) = \frac{1}{C}\int i_c(t)dt = \frac{1}{C}\int\left(-\frac{v_i(t)}{R}\right)dt = -\frac{1}{CR}\int v_i(t)dt$$

RC is the integration time constant

Transient analysis can be used to show that the circuit is marginally stable; this means that the circuit is not usable by itself, but it does form a vital building block in many types of system, including active filters

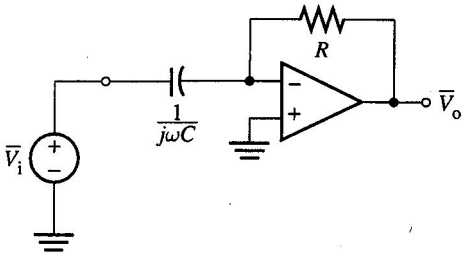
Example 15: Find the voltage gain function for the following circuit and sketch the Bode plot:



Solution

This circuit is related to the one in the last example by interchange of capacitor and resistor:

The phasor circuit is:



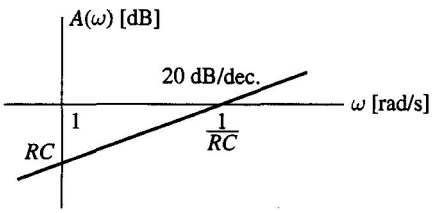
This circuit has the topology of the general inverting configuration shown above but Z_1 and Z_2 are interchanged

Hence, the voltage gain transfer function is:

$$\frac{\overline{V_o}}{\overline{V_i}} = H(j\omega) = -\frac{Z_2(j\omega)}{Z_1(j\omega)} = -\frac{R}{1/j\omega C} = -j\omega CR = \omega CR\angle -90^\circ$$

The phase is again constant (this time at – 90°), so we will not plot it

The gain function rises linearly at 20 dB/dec as shown:



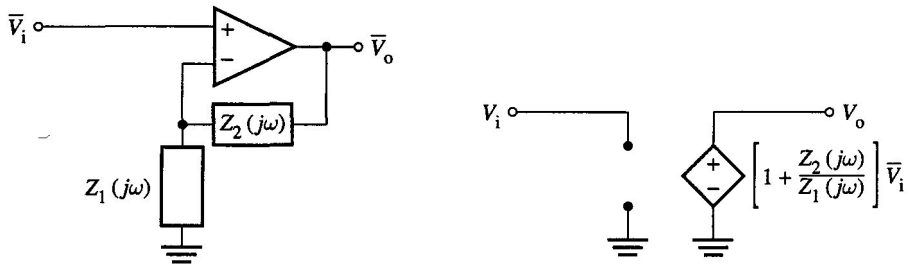
This circuit is referred to as a differentiator circuit; it may be shown that the output voltage is the differential of the input voltage

$$v_o(t) = Ri_R(t) = R\left(-C\frac{dv_i(t)}{dt}\right) = -CR\frac{dv_i(t)}{dt}$$

6.3 The non–inverting op-amp topology

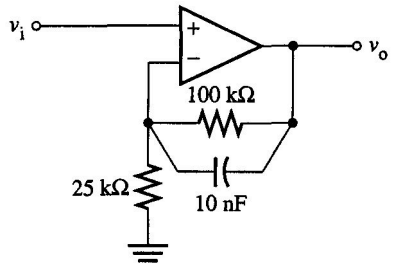
We showed that the inverting amplifier configuration which we analysed previously using resistors as elements could be generalised to the case of general impedances as elements

A similar generalisation is possible for the non-inverting configuration:



Note that for the non-inverting configuration, unlike the inverting configuration, the input impedance is infinite

Example 12.16: Find the voltage gain function v_o/v_i for the circuit shown and sketch the linearised Bode gain plot:



Solution

We first identify the circuit as having the non-inverting topology

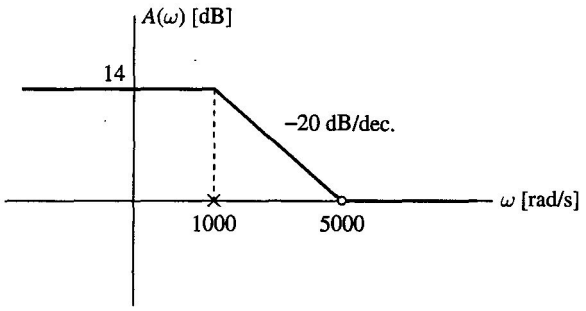
Next, we identify the two impedances: $Z_1(j\omega)$ corresponds to the 25 kΩ resistor and $Z_2(j\omega)$ to the 100 kΩ resistor and l0 nF capacitor connected in parallel:

$$Z_1(j\omega) = 25\times10^3 \qquad Z_2(j\omega) = \frac{10^5 \times \frac{1}{j\omega 10^{-8}}}{10^5 + \frac{1}{j\omega 10^{-8}}} = \frac{1}{j\omega 10^{-8} + 10^{-5}}$$

Next, we use the equivalent circuit for the non-inverting amplifier to write the voltage gain:

$$\frac{\overline{V_o}}{\overline{V_i}} = H(j\omega) = 1 + \frac{Z_2(j\omega)}{Z_1(j\omega)} = 1 + \frac{\frac{1}{j\omega\times10^{-8}+10^{-5}}}{25\times10^3} = \frac{j\omega\times10^{-3}+5}{j\omega\times10^{-3}+1}$$

The Bode gain plot is as follows:



Note here that the low frequency constant asymptotic gain is 20log(5) = 14 dB

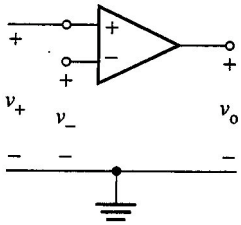
The high frequency constant asymptotic gain (well above 5000 rad/s) is 20log(1) = 0 dB

6.4 Frequency Response of the Op–amp Itself

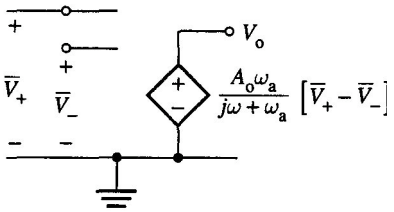
We have assumed so far that op–amp gain is independent of frequency, whether it is infinite (ideal op–amp) or a constant finite value

We now explore the practical case where the op-amp has a non-infinite, or finite, bandwidth

We start by showing the op-amp terminal voltages:



The current into each of the input terminals is always zero; therefore, it is equivalent to the open circuit shown in the phasor equivalent circuit:



This equivalent circuit for the op-amp includes the frequency response of the op–amp:

$$\overline{V_o} = H(j\omega)\left(\overline{V_+} - \overline{V_-}\right)$$

$$H(j\omega) = \frac{A_o}{1 + j\dfrac{\omega}{\omega_a}} = \frac{A_o\omega_a}{j\omega + \omega_a}$$

We can write the voltage frequency response function in Euler form:

$$H(j\omega) = \frac{A_o}{\sqrt{1 + (\omega/\omega_a)^2}} \angle \tan^{-1}(\omega/\omega_a)$$

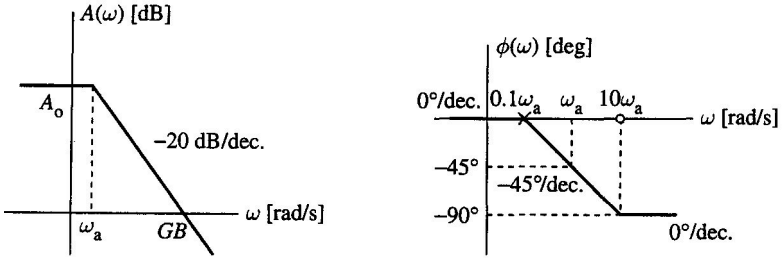
For $\omega \to 0$, we have:

$$|H(j0)| = A_o$$

Thus A_o is the low frequency constant gain asymptote, or simply DC gain

Fo $\omega = \omega_a$, the real and imaginary parts in the denominator become equal defining a break frequency as the gain begins to follow a –20 dB/decade asymptote of falling gain at higher frequencies

The gain and phase asymptotes for the op-amp are as follows:



For the most common type of op-amp called the 741, the magnitudes of the parameters are:

$$A_o \approx 10^5 \qquad f_a = \frac{1}{2\pi}\omega_a \approx 10 \text{ Hz}$$

The model for the frequency response is a simple RC lowpass filter type of response called the dominant pole model; in practice, most op-amps follow this characteristic quite well

We consider now the high frequency asymptote in more detail; let $\omega \to \infty$ in the op-amp frequency response function:

$$\left|H(j\omega)\right|_{\omega\to\infty} = \frac{A_o\omega_a}{\omega}$$

This expression describes the high frequency –20 dB/decade asymptote

The frequency ω at which this asymptote reaches a gain of unity (or 0 dB) is called the unity gain cut-off frequency and designated GB or ω_T

From the above, we have:

$$\omega_T = A_o\omega_a$$

Because A_o is the low-frequency (or DC) voltage gain and ω_a is the 3 dB bandwidth, ω_T is also called the gain bandwidth product

Sometimes one uses the Hertz form

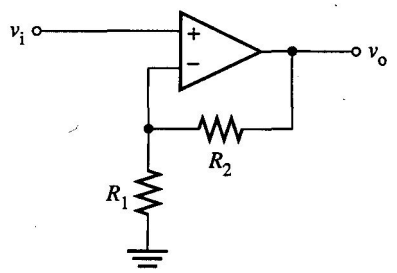
$$f_T = A_o f_a = \frac{\omega_T}{2\pi}$$

For the 741 type of op-amp, we have typically:

$$f_T = A_o f_a = 10^5 \times 10 \text{ Hz} = 10^6 = 1 \text{ MHz}$$

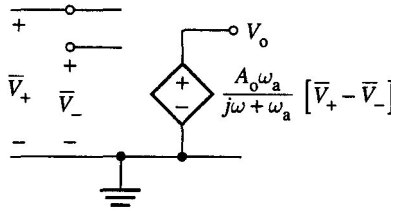
Example 17

Find the voltage transfer function for the non-inverting op-amp circuit shown and sketch the Bode gain plot assuming that the op-amp can be represented by its dominant pole model:

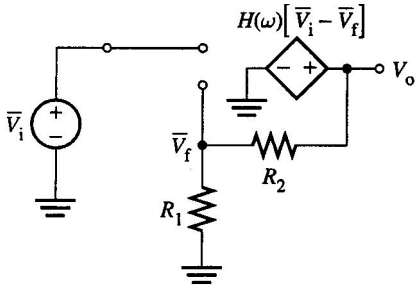


Solution

We first replace the op-amp symbol with the non-ideal op-amp model:



This results in the phasor equivalent circuit shown:



Analysis can proceed using KCL and the voltage divider rule, but in this case we define a feedback factor:

$$F=\frac{R_1}{R_1+R_2}$$

and obtain:

$$\overline{V_o}=H(\omega)\left(\overline{V_i}-\overline{V_f}\right)=H(\omega)\left(\overline{V_i}-F\overline{V_o}\right)$$

Thus:

$$\overline{V_o}=\frac{H(\omega)}{1+FH(\omega)}\overline{V_i}$$

We next insert the explicit equation for H(ω); this results in:

$$\overline{V_o}=\frac{1}{1/H(\omega)+F}\overline{V_i}=\frac{1}{(j\omega+\omega_a)/A_o\omega_a+F}\overline{V_i}=\frac{A_o\omega_a}{j\omega+\omega_a+FA_o\omega_a}\overline{V_i}=\frac{A_o\omega_a}{j\omega+(1+FA_o)\omega_a}\overline{V_i}$$

This leads to the closed loop voltage transfer function G(jw)

$$G(j\omega)=\frac{\overline{V_o}}{\overline{V_i}}=\frac{A_o\omega_a}{j\omega+(1+FA_o)\omega_a}$$

We express this in a form similar to that of $H(j\omega)=A_o\omega_a/(j\omega+\omega_a)$:

$$G(j\omega) = \frac{\frac{A_o}{1+FA_o} \times (1+FA_o)\omega_a}{j\omega + (1+FA_o)\omega_a} = \frac{G_o \omega_a'}{j\omega + \omega_a'}$$

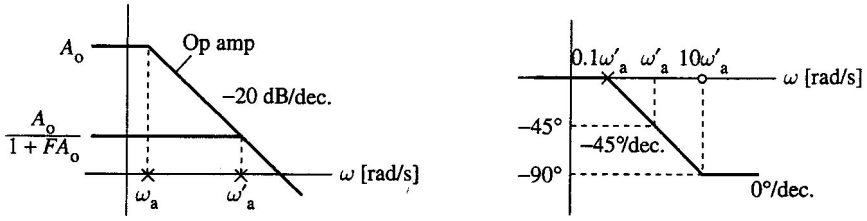
where Go is the closed loop DC gain:

$$G_o = \frac{A_o}{1+FA_o} \approx \frac{1}{F}$$

and ω_a' is the closed loop bandwidth:

$$\omega_a' = (1+FA_o)\omega_a \approx FA_o\omega_a \approx \frac{A_o}{G_o}\omega_a \approx \frac{\omega_T}{G_o}$$

We can immediately see that the gain of the op-amp itself has been reduced and the bandwidth increased both by the same factor:



We have superimposed a plot of the open loop gain (the gain of the op-amp itself) over the gain plot of the complete amplifier to allow comparison

Since the gain of the op-amp has been reduced by the same factor that the bandwidth has increased, this means that corner point for the closed-loop response will always lie on the –20dB/dec asymptote of the open-loop op-amp gain curve, as shown

The variable in the design is the feedback factor F which depends on the ratio of the resistors

For small values of F, the gain will be high and the bandwidth small; for high values of F, the gain will be low and the bandwidth high; in all case, the corner point will lie on the amplifier's –20 dB/dec asymptote

We can see now how op-amp circuits can possess a reasonably high bandwidth even though the bandwidth of the op-amp itself may be as low as 10 Hz

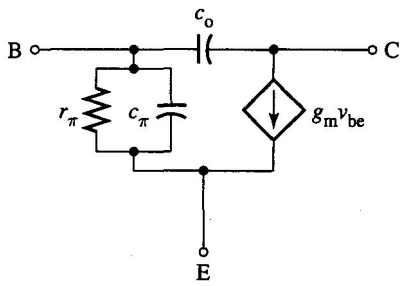
For example, for the 741 op-amp, possible closed-loop gain and bandwidth combinations are as follows:

G_o	f_a'
1	1 MHz
10	100 kHz
100	10 kHz
1000	1 kHz

If the bandwidth for a given gain requirement is not high enough, then a special wideband op-amp would have to be used.

7 FREQUENCY RESPONSE OF THE BJT

A popular model for the BJT that includes frequency effects is the hybrid–π model:



It is obtained from the DC hybrid–π model by adding two capacitances c_π and c_o

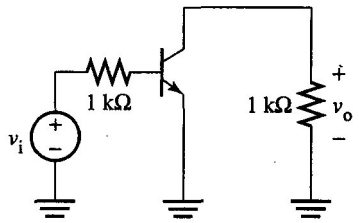
For operation in common-emitter mode, c_π is an input capacitance and c_o is a feedback capacitance (from output to input)

Resistors r_π and g_m and capacitors c_π and c_o are strictly functions of the instantaneous currents in the transistor

However, we work with a small signal model with constant parameter values valid for the DC bias point chosen

We consider an example circuit:

Example 19: Find the voltage transfer function for the small signal BJT circuit shown and sketch the Bode gain plot:

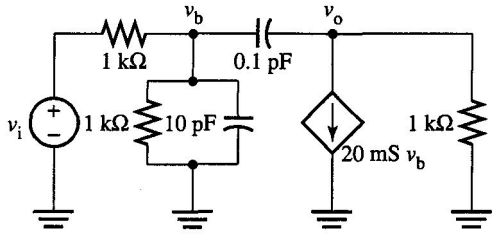


Assume that the BJT is well represented by its high frequency hybrid–π model with the following parameters which are valid at the chosen bias point:

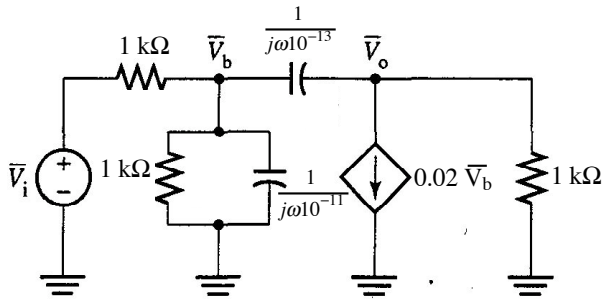
$$r_\pi = 1\ \text{k}\Omega,\ c_\pi = 10\ \text{pF},\ c_o = 0.1\ \text{pF},\ g_m = 20\ \text{mS}.$$

Solution

We replace the BJT symbol with the high-frequency small signal hybrid–π model, resulting in the time-domain equivalent circuit shown:



The phasor equivalent circuit is as follows:



There are two nodes $\overline{V_b}$ and $\overline{V_o}$ where KCL should be applied:

$$\frac{\overline{V_b}-\overline{V_i}}{1000}+\frac{\overline{V_b}}{1000}+\left(j\omega 10^{-11}\right)\overline{V_b}+\left(j\omega 10^{-13}\right)\left(\overline{V_b}-\overline{V_o}\right)=0$$

$$\frac{\overline{V_o}}{1000}+\left(j\omega 10^{-13}\right)\left(\overline{V_o}-\overline{V_b}\right)=-0.02\overline{V_b}$$

These simultaneous equations can be solved to obtain H(ω):

$$H(\omega)=\frac{\overline{V_o}}{\overline{V_i}}=\frac{0.1(j\omega'-200)}{(j\omega')^2+12.3(j\omega')+2}$$

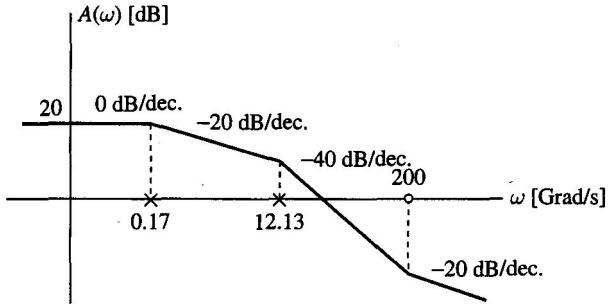
where ω' = ω/10^9, in other words ω' is in Grad/s units

In order to determine the Bode plot we must factor the denominator polynomial

In general, this requires a calculator or a computer but for the 2nd-order one as in this case, we can use the quadratic formula or complete the squares:

$$H(\omega)=\frac{\overline{V_o}}{\overline{V_i}}=\frac{0.1(j\omega'-200)}{(j\omega'+0.17)(j\omega'+12.13)}$$

The gain plot is as follows:



8 CONCLUSIONS

In this topic, we have given an introduction to circuits containing op-amps and transistors. We introduced the nullor equivalent for the ideal op-amp and considered nodal analysis of circuits containing op-amps. We considered practical aspects of op-amps circuits, including feedback and stability. We then looked at models for transistors. Finally, we considered the frequency response of op-amp and transistor circuits containing capacitors including a look at the frequency response of the op-amp itself.